**Course Title: Digital Logic and System Design**

**Course Code: CSE 210**

**Credit Hour: 1.5**

**Experiment No. 8**

**Experiment Name:**

a) Design and verify MOD 8 asynchronous up counter.

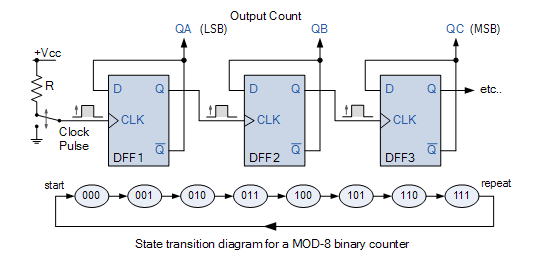
b) Design and verify MOD 8 asynchronous down counter.

c) Design and verify MOD 8 asynchronous up/down counter.

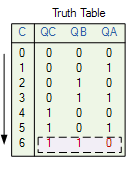
d ) Design and verify MOD 10 asynchronous up counter.

**Tasks:**

**MOD 8 asynchronous up counter:**



**Truth table:**

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|  |  |
| --- | --- |
| **000** | **111** |
| **001** | **110** |
| **010** | **101** |
| **011** | **100** |
| **100** | **011** |
| **101** | **010** |
| **110** | **001** |
| **111** | **000** |

|  |  |
| --- | --- |
| **0** | **0000** |
| **1** | **0001** |
| **2** | **0010** |
| **3** | **0011** |
| **4** | **0100** |
| **5** | **0101** |
| **6** | **0110** |
| **7** | **0111** |
| **8** | **1000** |
| **9** | **1001** |
| **10** | **1010** |

**Report:**

1) Problem Statement

2) Instruments (used in this experiment)

3) Logic diagram and Truth table

4) Discussion